



Operator's Manual

MODEL TR8828 SERIES AND
MM8103A, MM8104 or MM8105
TRANSIENT RECORDER SYSTEM



LeCroy

Innovators in Instrumentation



GENERAL INFORMATION

PURPOSE

This manual is provided to provide instructions regarding the use and operation of the transient recorder. In addition, it describes the theory of operation and provides information regarding the recording and application.

MODEL TR8828 SERIES AND MM8103A, MM8104 or MM8105 TRANSIENT RECORDER SYSTEM

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It is recommended that the manual be carefully inspected immediately upon delivery. All material in the manual should be checked against the equipment before use and changes reported promptly. If the manual is damaged in any way, please notify the Customer Service Department or the local field service office. If the manual is lost or deteriorating beyond repair, it may be replaced at no charge by requesting the writer in filling a change order.

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PRODUCT AVAILABILITY

Leaky is qualified concerning installation, calibration, and use of Leaky equipment are available from the Customer

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GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

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A T T E N T I O N

THE HIGH POWER DISSIPATION OF THIS MODULE REQUIRES THAT IT BE WELL COOLED. BE SURE FANS MOVE SUFFICIENT AIR TO MAINTAIN EXHAUST AIR TEMPERATURE TO LESS THAN 50° CELSIUS. DO NOT INSTALL MODULE IN FURTHEST LEFT SLOT OF CRATE, AS COOLING IS OFTEN LESS EFFICIENT THERE.

PROPER INSTALLATION OF THE MEMORY MODULES REQUIRES REMOVAL OF RESISTOR TERMINATORS FROM ALL MEMORIES EXCEPT THE ONE FURTHEST FROM THE TR8828 SERIES. SEE SECTION 1.2.3.6.

UNSOLDER ONE LEAD OF THE BATTERY OR REMOVE JUMPER E1-E2 BEFORE ATTEMPTING REPAIRS ON THESE MODULES.

ONLY MEMORY MODULES MM8103A AND MM8103 WITH HITACHI PART HM6116LP-2 MEMORY I.C.S OR MM8105 WITH HITACHI PART MM6264LP-12 CAN BE USED WITH THE TR8828 SERIES. MM8104 MEMORIES REQUIRE LECROY #205282116 OR SPECIAL SELECTED VERSIONS OF HM6116LP-2 MEMORY IC's. TR8828C's SHIPPED AFTER SEPTEMBER, 1985 WILL HAVE A MAXIMUM MEMORY SIZE OF 2 MEGABYTES INSTEAD OF 512 KILOBYTES.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION OR REMOVAL OF MODULE TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

A LATCH-UP CONDITION MAY OCCUR WHEN IN EXTERNAL CLOCK MODE. (SEE SECTION 1.2.3.3 PARAGRAPH 2).

SEE POCKET IN BACK FOR SCHEMATICS AND PARTS LISTS.

A T T E N T I O N

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TR8818A and TR8828C DIGITIZERS MM8103A, MM8104, MM8105 MEMORIES



- 100/200 MS/sec Digitizing Rate
- 100 MHz Bandwidth
- 8-Bit Resolution
- Long 32K to 2M Sample Records
- Programmable
- Modular, Expandable

FOR DIGITIZING AND RECORDING SIGNALS

LeCroy Models TR8818A and TR8828C are plug-in digitizers which provide the basic system core for high speed, long record waveform recording. The system modularity allows multiple channels, memory expansion, and mixing with other accessory modules or slower speed digitizers, thus providing flexibility for use in large and small system applications.

The two digitizers are identical except that the TR8828C digitizes at twice the rate (200 MS/sec) of the TR8818A and has a few additional features including burst mode, additional input ranges, and adjustable trigger. One digitizer along with one memory plug-in (MM8103A for TR8818A, MM8104 for TR8828C), mainframe and controller provide the minimum configuration for digitizing and recording high speed signals.

FEATURES

High Digitizing Rate — Maximum sampling rate of 200 MS/sec (5 nsec between points) for TR8828C or 100 MS/sec for TR8818A provides exceptional time resolution.

Wide Analog Bandwidths — The analog bandwidth of >100 MHz provides the ability to record high frequency signals while maintaining high signal fidelity.

Exceptional Accuracy — 8-bit resolution and low distortion provide high dynamic accuracy to preserve signal characteristics over the entire frequency range.

Large, Expandable Memory — From 32K to 2M sample points permit capturing signals with poorly correlated triggers, and allow the recording of fine detail on signals of long duration.

Memory Retention — Contents of data memory and control registers are internally battery backed-up for up to 1 year.

Time Base Clock In/Out — Permits operation with a clock from another digitizer or an external source.

Multiburst Capture — In Burst Mode, (TR8828C only) the memory accepts data only when enabled and can be used to store non-sequential waveforms of arbitrary length.

User Defined Trigger Controls — Adjustable slope and threshold level (TR8828C only) provide versatile triggering over ± 2 V range.

Versatile Pretrigger — Up to 100% of the memory may be allocated to pre-recording the waveform prior to the occurrence of the trigger.

Synchronization Outputs — Front-panel ARM and BUSY signals (TR8828C only) facilitate system coordination, and may be used to trigger other devices.

Programmable — Digitizers, and memory plug-ins may be externally controlled for automatic setup or unattended operation.

Compact — Suitable for benchtop operation or in configurations with up to 4 channels per rackwidth.

FUNCTIONAL DESCRIPTION

The Models TR8818A and TR8828C digitizers are optimized for digitizing and recording high frequency signals. This is evidenced by their wide bandwidth, fast sampling rate and most important, their high dynamic accuracy (i.e., "effective bits") even for signal frequencies approaching the Nyquist limit. Even the minimum system offers large memory capability, providing high frequency signal detail by allowing digitization over long periods. Moreover, the memory is easily expandable when it is necessary to record extremely long records.

The signal to be digitized may be connected directly to the 0.5 V full-scale input or via a modular amplifier (LeCroy 6102 or 6103) if gain control is required. The TR8828C also has a high level 5.0 V input which is internally summed with the normal input. In addition to accepting larger amplitude inputs, this allows algebraic addition of a timing marker, second analog signal or baseline correction.

Once armed by programmed command, the unit digitizes the input signal with 8-bit resolution and loads its associated memory. While the memory is being loaded, a FAST DAC (TR8828C only) reconstructs the data for user monitoring. This feature is useful in system testing and setup, and also may be used as an internal trigger.

The amount of memory is variable as determined by the number of memory plug-ins selected. With a TR8818A, single MM8103A or MM8105 memories provide storage for 32K or 128K samples respectively; up to 15 additional plug-ins can be added as required, providing up to 512K or 2M samples respectively. The same can be done with the TR8828C using the high speed MM8104 for single module operation, or MM8103A or MM8105 memory modules used in pairs. Up to 100% pre- and post-trigger recording is available.

The TR8828C also has a burst mode in which samples can be loaded into the memory only when the stop trigger signal is below the threshold level. This mode may be used to divide the memory into segments for multiburst recording; the user must provide externally generated segment markers to allow data reconstruction.

The programmable parameters (memory size, pretrigger sample size, sampling speed, and input offset) can be set or read at any time the unit is not digitizing. Complete control is available using the programmable arm (start digitizing) or stop trigger commands and the Look-At-Me flag (indicating data ready).

SPECIFICATIONS

SIGNAL INPUT

Amplitude Range: 510 mV p-p (2mV/lb) $\pm 1\%$ F.S., $\pm 0.1\%/^{\circ}\text{C}$
Impedance: 50 Ω $\pm 3\%$ DC; $< 7\%$ reflection from 3 nsec edge
Bandwidth: DC to > 100 MHz (-3 dB)
Offset: Programmable over $\pm 1/2$ full scale in 256 steps; tempco of $\pm 0.1\%$ F.S./ $^{\circ}\text{C}$ maximum
Overload Recovery: Recovers to $\pm 1\%$ of F.S. in 25 nsec from a $1.5\times$ overdrive pulse of < 1 μsec duration
Overload Protection: ± 2.5 V DC; ± 500 V for 30 nsec or ± 100 V for 100 μsec with 50 Ω source

HIGH LEVEL ($\times 10$) SIGNAL INPUT (TR8828C only)

All characteristics same as above except:

Amplitude Range: 5.10 V p-p (20mV/lb) $\pm 2\%$ F.S., $\pm 0.1\%/^{\circ}\text{C}$
DC Overload Protection: ± 7.5 V
Configuration: Internally summed with normal input

ANALOG TO DIGITAL CHARACTERISTICS

Resolution: 8 bit (offset binary code)
DC Accuracy: Errors are less than ± 1.5 counts plus $1/2$ count quantizing error from best linear fit over entire range.
AC Accuracy: A reconstructed digitized pure sine wave has a minimum dynamic accuracy as follows:

Signal Frequency	Signal Amplitude	Effective Bits	Sig/Noise Ratio(dB)
To 5 MHz	80%	6.5	39
5-20 MHz	80%	6.0	36
20-50 MHz	50%	6.0	32
50-100 MHz*	50%	5.5	29

*applies to TR8828C only

Aperture Uncertainty: ± 5 psec maximum
Noise: RMS Noise < 1.7 counts, not including misconversions. The probability of a misconversion (defined as > 3 counts) is typically ≤ 1 per million averaged over the entire amplitude range.

TIMEBASE

Internal: TR8818A, 100 MHz $\pm 0.01\%$ crystal oscillator and divider provide sampling periods of 10, 20, 40, 80, 160, 320 or 640 nsec; TR8828C, same except 200 MHz clock provides periods from 5 to 320 nsec.
External Clock: User clock can be supplied via 50 Ω front-panel connector. TR8818A, allows any clock rate to 100 MHz, ECL or TTL levels; TR8828C requires fixed 200 MHz ECL level only.

Clock Out: ECL level clock pulses available via front-panel connector.

STOP TRIGGER CHARACTERISTICS

Slope: TR8818A, + only; TR8828C, + or -, set at side panel.
Level: TR8818A, choice of TTL($+2.5$ V) or ECL(-1.2 V) set at side panel; TR8828C, variable from -2 V to $+2$ V, adjusted and monitored from front panel.
Impedance: 50 Ω $\pm 3\%$
Duration: 8 nsec minimum
Overload Protection: ± 2.5 V DC; ± 250 V for 1 usec with ≥ 50 Ω source.

Modes: In normal mode trigger switches from pretrigger to post-trigger sampling, digitizing stops when post-trigger sampling is complete. In Burst Mode (TR8828C only) segmenting of memory is achieved by disabling the memory clock for the duration of the input trigger pulses.

MEMORY

Options:	Size	Speed
MM8103A	32K	100/200 MS/sec*
MM8104	32K	200 MS/sec
MM8105	128K	100/200 MS/sec*

* MM8103 and MM8105 must be used in pairs when operated with the TR8828C

Active Memory Size: Programmable in 8K sample increments for TR8818A, 16K for TR8828C, up to the total size of memory installed (2M samples maximum if using MM8105 memory modules).

Pretrigger: Memory can be divided into pre- and post- trigger sample storage, programmable in increments of 1/8s of user acquisition memory.

Burst Mode (TR8828C only): Side-panel jumper option enables front-panel STOP trigger input to double as a memory clock control, allowing efficient use of memory when digitizing many short record segments. (Pretrigger and programmed stop features cannot be used.)

Battery Backup: Data in memory is preserved when external power is removed.

GENERAL

Connectors: TR8818A, all front-panel connectors are BNC; TR8828C, all front-panel connectors are BNC, except FAST DAC, ARM BUSY, TRIG BUSY, and CDS (manual control enable) which are Lemo. Cables with either BNC or Lemo connectors are available from LeCroy.

Status Lights: Front-panel LED's indicate power and digitizing status.

Module ID: 8-bit side-panel switch allows a unique user assigned module identification number which can be read to the dataway.

Power Requirements:

	± 6 V	-6 V	+24 V	-24 V
TR8818A	440 mA	7.8 A	221 mA	140 mA
TR8828C	900 mA	10.0 A	220 mA	175 mA
MM8103A	2.5 A	1.3 A	—	—
MM8104	2.5 A	1.3 A	—	—
MM8105	2.7 A	1.3 A	—	—

Internal Battery: Replaceable Lithium battery (lifetime > 2 years) in each memory module and digitizer automatically becomes power source for memory and control registers.

Environment: Proper operation requires $+15^{\circ}\text{C}$ to $+25^{\circ}\text{C}$ intake air with sufficient airflow to maintain temperature rise of exhaust air to $< 15^{\circ}\text{C}$ ($+30^{\circ}\text{C}$ intake air allowed if sufficient airflow to maintain temperature rise of exhaust air to $< 10^{\circ}\text{C}$).
TR8818A only: Identical. Specifications and performance may degrade slightly with temperature.
Operating humidity range up to 90% relative humidity non-condensing at $+25^{\circ}\text{C}$
Operating altitude $< 10,000$ ft above sea level ($< 3,045$ meters).
Non-operating temperature range is -10°C to $+50^{\circ}\text{C}$.

Packaging: RF shielded module in conformance with the CAMAC (IEEE 583) Standard.

	Size	Height	Width	Depth
TR8818A	#2	221 mm	34 mm	292 mm
TR8828C	#3	221 mm	51 mm	292 mm
Memories	#1	221 mm	17 mm	292 mm

PROGRAMMABILITY AND READOUT

All programmable waveform recorder parameters can be set or read and the recorded data can be read by a controller or a computer. This may be accomplished via any mainframe interface such as the LeCroy Model 8901A or 6010 GPIB (IEEE 488) Interface. Other interfaces compatible with the CAMAC (IEEE 583) Standard may be used.

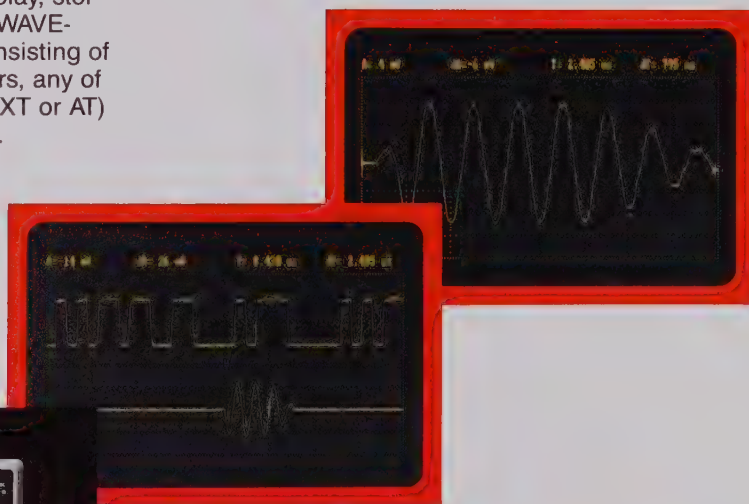
WAVEFORM-CATALYST

The TR8818A or TR8828C and its associated memory modules are fully compatible with LeCroy's WAVEFORM-CATALYST, a multichannel digital oscilloscope with powerful capabilities for acquisition, display, storage, and analysis of high-speed waveforms. WAVEFORM-CATALYST is an integrated system consisting of LeCroy's series of modular waveform digitizers, any of the IBM™ personal computers (PC, Portable, XT or AT) and system WAVEFORM-CATALYST software.

MAINFRAMES AND ACCESSORIES

The LeCroy 8013A benchtop 13-slot mainframe will house and power two TR8818A's with up to three memories each or two TR8828C's with one memory each. For rack mounting and/or greater numbers of channels, the LeCroy 1434A rackmount 25-slot powered mainframe can be used.

LeCroy offers other accessory modules such as dual channel amplifier/trigger generators (Model 6102 100 MHz manual and Model 6103 150 MHz programmable). Also available are various clock, time and gate generator modules. Please call our application engineering staff for further information.



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SECTION 1

1.1.1 Programming and Readout Commands

All CAMAC Dataway commands listed below except F(25) are disabled during conversion. To prevent possible noise induced by asynchronous digital switching, it is recommended that no unnecessary CAMAC commands be generated on the Dataway during the actual analog to digital conversion cycles (i.e., between arming units and receiving a LAM).

The Z (Initialize) command from the CAMAC dataway will clear and disable all Look-At-Me's (LAM's) and disable (unarm) the A-D converter, but will not otherwise affect control registers or stored data. All CAMAC function codes respond to A(0) only. An X- and Q-response is returned for all valid commands except a Q-response requires that a valid data transfer has occurred (on a read or write command) or that the appropriate LAM is present (on a F(8) or F(27) command).

Parameter Setup, Status and Control Commands:

Input Offset: F(1) reads from R9-R16; F(19) writes to W1-W16. Data is 8-bit binary representation of the input offset voltage where offset = 255 - N mV for N = 0 to 255.

Control Register: F(0) reads from R1-R16; F(16) writes to W1-W16. Data is 16-bit binary word, bit coded as follows:

W/R15-W/R9 Memory Samples (X 1024)		W/R7-W/R5 Sampling Period (nsec)		W/R4-W/R1 Pretrigger Samples (fraction of active memory)	
0	16	0	5	0	0/8
1	32	1	10	1	1/8
2	48	2	20	2	2/8
3	64	3	40	3	3/8
4	80	4	80	4	4/8
5	96	5	160	5	5/8
.	.	6	320	6	6/8
.	.	7	EXT	7	7/8
127	2048	200 MHz only		8	8/8

W/R8 is not used; W/R16 is available to the user for storing programmable identification flag bit or event related information. Writing or reading it does not effect any other module parameter.

Trigger Arm: F(9) will arm unit, and if internal clock is used, start digitizer, allowing the next trigger to initiate digitizing stop cycle. If the external clock is selected, F(9) will enable the clock input, but then requires an external clock to digitize and respond to a Trigger or F(25). All

other commands are disabled when in the Armed stated.

Internal Trigger: F(25) generates an internal trigger (OR'd with external trigger input). Used in auto-trigger modes or when calibrating, testing or demonstrating when no external trigger is available.

Module ID Word: F(3) reads an 8-bit binary value from user settable switch on R1-R8.

Memory Access Commands:

Enable Read Mode: F(17) sets address counter to beginning of data record. Must be followed by F(2) or Z.

Digitized Data: F(2) reads two 8-bit samples on R1-R16 from the current memory location, then increments memory address by one. The two 8-bit samples contained in each 16-bit word are in binary representation, lower byte first. The first byte is the time vernier, see below. The next 15 bytes and the last 16 bytes may be inaccurate and therefore should be discarded. Must be preceded by F(17) command (Enable Read Mode) to set address counter to beginning of data record. Q=1 while memory data is valid, going to 0 after last data word.

Trigger Time Vernier:

The high speed nature of the digitizer requires that four samples be simultaneously transferred to memory. R1 and R2 of first byte specifies which of the four bytes (of the next two words) starts the data record as follows:

R1-R2	First Sample
0	R1-R8 of 1st word
1	R9-R16 of 1st word
2	R1-R8 of 2nd word
3	R9-R16 of 2nd word

Note that even though this defines the location of the first sample, the actual data may be inaccurate until the 17th sample (9th word) is read.

LAM Commands:

The LAM line on the CAMAC dataway indicates that a stop Trigger has occurred and all post-trigger samples have been stored in memory.

Test LAM Status: The status of LAM also can be checked by F(8) or F(27) where a Q=1 response indicates that LAM is present. F(8) requires that LAM Enable be set.

Enable LAM: F(26) will allow LAM x to drive CAMAC dataway LAM line.

Disable LAM: F(24) will not allow LAM x to drive CAMAC dataway LAM line. Z or C will Disable both LAM's.

SPECIFICATIONS

1.2 System Description

1.2.1 Introduction

The transient recorder system is modular and is comprised of two or more modules. The TR8828 Series is the analog-to-digital converter (ADC) and control module. Two MM8103A or two high density MM8105 memory modules per TR8828 Series are used in a "ping-pong" fashion to achieve the speed necessary for system operation or one high speed MM8104 may be used. Up to 64 MM8103A or 16 MM8105 modules can be used with the TR8828 Series transient recorder, giving a maximum memory size of 2 megabyte samples.

The limited application MM8104 memory is a special high speed version of the MM8103A allowing use of a single 32K module with the TR8828 Series. While the cost of the high speed memory IC's makes the cost/sample high, this may be justified by the power and crate volume savings when memory size is not required. The MM8104 can be made to look like and be used with MM8103A units by changing a side-panel jumper, thus economical system expansion is easily done. Throughout the rest of this manual, the MM8104 will be referenced only when there is a difference in operation between it and the MM8103A/MM8105.

These modules plug into a CAMAC crate (see IEEE Standard. 583-1975) and follow the CAMAC instrumentation and interface standards. A minimum system consists of one triple-width TR8828 Series and two single-width MM8103A/MM8105 (or one single-width MM8104) CAMAC modules. Two cables, a 34-conductor and a 50-conductor, connect the three modules electrically.

An analog signal of amplitude less than 512 mV is digitized by the TR8828 Series at a rate determined by the clock. The digitized signal is stored sequentially in the memory modules. After receipt of the stop command and post-trigger interval, the data can be read sequentially from the memory modules via control signals from the TR8828 Series. All control registers in the TR8828 Series and the memories in the memory modules have an auxiliary battery supply which retains the data when the power is off.

The source of the clock and stop, the post-trigger interval, and the active memory size can be selected by the appropriate CAMAC command. Other options can also be programmed as indicated in the data sheet.

This system can be controlled by any computer that has access to the CAMAC crate through a crate controller. The modules require some type of crate controller for operation.

1.2.2 General Description

The TR8828 Series and memory make up a 200 megasample/sec transient recorder. The TR8828 Series transient recorder converts an analog input signal into 8-bit digital words at a sampling frequency of 200 MHz. Each MM8103A/MM8104 memory module stores up to 32768 (32K) 8-bit samples (bytes) or 131072(128K) for MM8105 memory generated by the TR8828 Series. From 1 to 64 memory modules can be used with the transient recorder thus storing a maximum of 2 megabytes of data. The transient recorder and memory module are standard CAMAC modules. The transient recorder requires three slots while each memory requires one. The CAMAC dataway provides computer control of the system.

Figure 1.1 contains a block diagram of the system showing the general components. The analog input is first offset by the amount specified in the 8-bit offset register. The CAMAC dataway reads and writes to this register using F(1) and F(19) CAMAC functions. After being offset up to ± 255 mV, the input signal is digitized into an 8-bit offset binary code. A fast digital-to-analog converter regenerates these digitized samples and drives a front-panel output so the user can view the input signal without storing it in the memories during setup.

A portion of the control register specifies the sampling frequency of the analog-to-digital converter. The CAMAC dataway reads and writes to the control register using F(0) and F(16). Thus, one of seven internal sampling frequencies from 3.2 to 200 MHz or an external 200 MHz clock may be chosen as the sampling frequency. The transient recorder provides the 200 MHz clock as a front-panel output. The transient recorder starts sampling when an F(9) function is received and stops when either an F(25) is received or the front-panel input, stop trigger, detects the selected edge. The external clock must be 200 MHz ± 1 MHz.

Once digitized, the data is stored in the memories. The control register also specifies how this is done with the pretrigger and memory size portions of the control word. When sampling starts, the memory begins storing data in a circular fashion. The transient recorder fills the memory sequentially. Upon reaching the end of memory as set by the control word, the transient recorder starts again at the beginning and writes over the old data. The transient recorder continues in this manner until it receives a stop signal. After the stop signal, the control logic subtracts the amount of pretrigger specified in the control word from the memory size. This number determines how many additional samples are stored after the stop signal. After the last sample is stored, the next address is saved to locate the start of the recorded data. When the transient recorder finishes storing data, it generates a LAM signal. The functions F(8) and F(27) test for the presence of the LAM.

After detecting the LAM, the computer controller may read the recorded data by generating the function F(17), which sets the memory address counter to the starting address of the data record. Then, the function F(2) will read the data 2 bytes at a time. When the entire record has been read, the Q response for the F(2) will change from 1 to 0.

1.2.3 Detailed Information

1.2.3.1 Control Register

The control register is 16 bits in length and programmable via the CAMAC dataway using F(16) and A(0) with W1 through W16. Asserting F(0) and A(0) on the CAMAC dataway will enable the control register onto R1 through R16. The control register contains the user bits, memory size, sampling period, and pretrigger size in the following format.

W16 . . .	W1
R16 . . .	R1
U2 M6 M5 M4 M3 M2 M1 M0 0 S2 S1 S0 P3 P2 P1 P0	

Where: U0 is a user bit

M0, . . . M6 is the memory size

S0, S1, S2 is the sampling period

P0, . . . P3 is the pretrigger size

The control register is decoded as follows:

M0-M6		S0-S2	P0-P3	
			0	0/8 of active memory
0	16k bytes	0 5 nsec	1	1/8
1	32k bytes	1 10 nsec	2	2/8
2	48k bytes	2 20 nsec	3	3/8
3	64k bytes	3 40 nsec	4	4/8
.		4 80 nsec	5	5/8
.		5 160 nsec	6	6/8
.		6 320 nsec	7	7/8
127	2048k bytes	7 external clock (200 MHz only)	8	8/8

Only the bits for valid functions of the sampling period and pretrigger will be stored and read back. P0, P1, and P2 will read back as 0 if P3 is written as a 1.

P0-P3 set the pretrigger size, the fraction of the selected memory size that will precede the stop command. For example, if a memory size of 32K and a pretrigger size of 3/8 are selected, then after a digitizing cycle, the first 12k bytes of memory will contain data sampled just prior to the stop command and the last 20k bytes just after the stop command.

S0-S2 set the period of the sampling clock. As shown above, one may choose any of seven internal periods or an external period of 5 nsec. The external clock should have a 50% duty cycle.

M0-M6 set the size of the data record. These bits select any memory size from 16K to 2M in 16K increments.

The user bit U0 can be set and read and is maintained during power down. This bit has no internal function so it can be used for storing status, run number, etc. by the user.

1.2.3.2 Offset Register

Analog signals at the input to the TR8828 Series may be offset by ± 255 mV with the offset register. The offset register is 8 bits in length and is programmed via the CAMAC dataway. Asserting F(19) and A(0) will write W1 through W8 to the offset register. Asserting F(1) and A(0) will read back the offset register in R9 through R16.

Writing 0 to the offset register allows input signals between ground and -510 mV to be digitized. An offset of 127 allows signals between -255 mV and $+255$ mV to be digitized. An offset of 255 allows signals between ground and $+510$ mV to be digitized. Intermediate values of offset will displace the input signal correspondingly.

On units shipped after May 1, 1984 the offset circuitry is factory calibrated so that the actual offset will differ from the programmed request by less than $\pm 2\%$ of full scale (± 5.0 counts). If 2% accuracy is not sufficient, the user can always obtain the exact number of offset counts desired. This can be done by writing an offset, reading back the actual offset and then adjusting the requested offset a few counts to obtain the desired final offset.

For applications in which highest precision is needed, the user should be aware that the DC level of the input can have some effect on accuracy. If the input is biased to the exact center of full scale then it will

toggle between outputs of 10000000 and 01111111. This situation (with all bits toggling) will generate enough noise to occasionally cause other readings. In all cases it is guaranteed that the rms variation of the output will be less than two counts but typically the rms variation is less than one count. In order to avoid the possible inaccuracy introduced by this effect it is recommended that the user not apply a DC level to the input (or request an offset) corresponding to 127 counts. Similar but smaller effects may be observed at a few other DC input levels which correspond to the toggling of many bits (e.g. 63 and 191 counts). Units are factory checked using a test which averages 1000 samples at each of 1000 DC level inputs (total of 1 million samples). The 1000 DC levels cover a range of 500 mV to insure that nearly the full scale of the unit is sampled. When running this test, "conversion errors" (very rare bit errors discussed in Section 1.2.3.4) are identified first and the remaining samples are used to determine the rms noise level.

1.2.3.3 Data Readout

Digitized analog data is stored in the memory modules. The digitizing sequence is started by asserting F(9) and A(0) on the CAMAC dataway. While digitizing, the TR8828 Series is considered to be in the ready state. Only the stop command F(25) and A(0), the Stop input, or the initialize signal Z can remove the TR8828 Series from the ready state. Only one CAMAC function code command will be recognized, i.e. F(25) and A(0). All others will be ignored and will generate Q=0.

When operating in the external clock mode, a stop trigger will not be recognized unless an external clock is being supplied. Until this occurs, unit will disable all CAMAC commands and effectively be "hung-up".

After receipt of the stop command, the post-trigger samples will be acquired, the ready state will be negated, and the internal LAM will be set. If the internal LAM is enabled via F(26) and A(0), LAM will be asserted on the dataway. LAM can be cleared via F(10) and A(0) or Z. Asserting F(9) and A(0), starting a new digitizing cycle, will also clear the LAM.

The LAM indicates the completion of the digitizing sequence. Digitized data can be read from the memory modules via commands sent to the TR8828 Series. Asserting F(17) and A(0) will load the starting address of the data in memory from an internal register into the address counter. The data can then be read by generating successive F(2) and A(0) commands. Q will be true (Q=1) for every valid data sample. After the

last sample is read, further F(2) and A(0) commands will produce Q=0. The data can be read again by asserting F(17) and A(0) to reload the starting address and then using F(2) and A(0) to read the Data.

Data is read sequentially from the memory modules 2 bytes at a time. R1-R8 contain the first byte in each pair. R9-R16 contain the second. This maximizes the transfer rate to the computer. The first word (R1-R16) that is read with F(2) and A(0) after F(17) and A(0) is a status word. If this word is zero, the first byte R1 - R8 of the next word is the first byte of the data record. If the status word is a one, the second byte R9 - R16 of the next word is the first byte of the data record, etc. See Section 1.2.3.7 for complete details of the data readout procedure. Because the data bytes are pipelined into the memory, the first and last 16 bytes of the data record will be garbled.

The reliability of data is carefully checked by the factory. Prior to shipment all units undergo thorough testing including operation for several days at the maximum specified temperature. Some tests include the input of slow ramp signals and many frequencies of sine waves. The output is then compared with the known input. On very rare occasions a single data word will have a bit error. A particular bit which should be on may be off or vice-versa.

This type of error may be found in all systems which use flash ADC's near their maximum conversion rate. These conversion errors (also sometimes called "Flyers") will result in wrong information on one or more bits from the ADC. All units are factory checked for a conversion error rate. Typically it is less than one wrong data sample per 32,000 data words using the 1 million sample test discussed in Section 1.2.3.2.

1.2.3.4 ID Word

Asserting F(3) and A(0) causes the 8-bit identification word to be read via R1-R8 of the CAMAC dataway. A switch array accessible from the bottom edge of the module allows convenient changing of the ID word. At calibration the ID word is set to the binary-coded decimal representation of the last two digits of the serial number.

1.2.3.5 Battery Backup

Lithium chloride batteries are used to back up all important registers in the TR8828 Series and the memory modules. Registers for control and starting

address in the TR8828 Series and memories in the memory modules are maintained by these batteries when the power is off. The batteries are not recharged when power is applied. In the backup mode (power off) battery lifetime is in excess of two years, typically 5 - 10 years at 25°C. The batteries are replaceable.

1.2.3.6 Memory Modules

Each MM8103A or MM8104 module can contain 32k bytes of digitized data. Each MM8105 can contain 128k bytes of digitized data. The memory size programmed into the TR8828 Series determines the amount of active memory. Address and data are sent to the memory module(s) from the TR8828 Series. The 34-pin connector has the signal lines necessary to tell the memory where to write or read the data. On a write cycle the memory module gets 4 bytes of data at a time from the 50-pin connector and writes them to memory. A read cycle causes the memory module to read 2 bytes as specified by the address and to present those 2 bytes to the CAMAC dataway on R1 through R16.

A 6-position switch on the front panels of the memory modules indicates the starting address of the 32k bytes of memory in the module. Two MM8103A modules with a TR8828 Series should have switches (SW) 1 thru 5 in the closed or zero address position. One of the two modules in a pair should always have SW 6 open and the other with SW 6 closed. Adding a second pair of modules requires that the second set of switch registers be set to an address of one, i.e., SW 1 open, SW 2 - 5 closed. Again, one of the pair should have SW 6 open and the other SW 6 closed. A third pair of modules would be set to an address of two, i.e., SW 1 closed, SW 2 open, SW 3 - SW 5 closed. Fourth module would be set to an address of three, i.e., SW 1 opened, SW 2 opened, SW 3-SW 6 closed, etc. The address space of the TR8828 Series limits the number of memory modules to 64 or 2 megabytes of memory. SW 4 and SW 5 will not be moved from the closed position.

If a single MM8104 module is used, all switches (SW) 1 through 6 should be in the closed position. If the side-panel jumper is put in the 8103 position, then the MM8104 can be used as a MM8103A, following the switch rules in the previous paragraph.

MM8105 operates in the same way as the MM8103A except it has a 4-position switch. SW 1 thru 3 act in the same manner as SW 1 thru 5 for MM8103A and SW 4 is the same as SW 6. The address space of the

TR8828 Series limits the number of modules to 16, or 2 megabytes of memory. This is the same limit as the MM8103A but in less modules.

Each memory module has resistor terminators for the front-panel cables. The module furthest from the TR8828 Series must be the only one with resistor terminators. Every module between the TR8828 Series and the furthest module should have seven single in-line resistor packages and one 100 Ω 1/4 W resistor removed. The seven SIP's and one 100 Ω resistor are socketed and can easily be removed through the cutout in the side panel. Note that the SIP's have an orienting mark on one end. See Figure 1.2 for proper orientation of SIP's.

The red/green LED at the top of the module indicates the status. Red indicates the module is receiving power from the CAMAC dataway and that all fuses are conducting. A blown fuse will turn off the red LED and will pull up one line on the 50-pin connector to -0.8 V. The TR8828 Series will respond to this power-fail indication by not returning an X response for any command.

Green will be flashed any time the memory module is accessed for a read or a write. The signal that drives the green LED is not stretched, causing the LED to flash only for the time the module is accessed.

1.2.3.7 CAMAC Command Summary

All CAMAC commands require N and A(0) to function. Every command described below will return an X=1 response unless one of the modules in the system is not receiving power, then a X=0 response is returned.

CAMAC commands will return a Q=1 response unless otherwise indicated below. A TR8828 Series in the digitizing or ready state will return a Q=1 response only for F(25). All other function code commands are ignored.

X: X=1 for all valid F commands with A(0) and N.
X=0 if power fails.

Q: Acknowledges the acceptance of the command.
The specific responses of each function are listed below.

- L: A LAM is generated at the end of the sampling sequence, if enabled by F(26). An internal LAM is always set at the end of the sampling sequence.
- Z: Resets the module. Clears and disables LAM; does not affect memory or control registers. Z should be asserted after power-up.
- F(0): Reads control register pretrigger size (R1-R4), sampling period (R5-R7), active memory size (R9-R15), and user bits (R16).

R9-R15 Memory Size	R5-R7 Sampling Period	R1-R4 Pretrigger
0 16K	0 5 nsec	0 0/8 of active memory
1 32K	1 10 nsec	1 1/8
2 48K	2 20 nsec	2 2/8
•	3 40 nsec	3 3/8
•	4 80 nsec	4 4/8
•	5 160 nsec	5 5/8
127 2048K	6 320 nsec	6 6/8
	7 EXT CLK	7 7/8
	(200 MHz only)	8 8/8

- F(1): Read offset register (R9-R16).
- F(2): Read the waveform data in 16-bit words. The first word, a status word, specifies which byte of the next two data words starts the data record. If the status word is a 0, R1-R8 of the first data word is the first data byte and R9-R16 is the second byte. If the status word is 1, then R9-R16 is the first data byte, and R1-R8 of the next data word is the second data byte. If the status word is 2 the first data byte is R1-R8 of the second data word read. A status word of 3 indicates that the first data byte is R9-R16 of the second data word read. Q=0 after the last data word is read.
- F(3): Read module identifier (R1-R8).
- F(8): Test LAM. Q=1 if LAM is set and enabled.

F(9): Set unit in Ready state, clear LAM, and start digitizing if the internal clock is used. If the external clock is selected, enable the sampling clock. Q=1 if not in Ready state.

F(10): Clear LAM.

F(16): Write to control register, pretrigger size (W1-W4), sampling period (W5-W7), memory size (W9-W15), and user bit (W16).

W9-W15 Memory Size	W5-W7 Sampling Period	W1-W4 Pretrigger
0 16K	0 5 nsec	0 0/8 of active memory
1 32K	1 10 nsec	1 1/8
2 64K	2 20 nsec	2 2/8
•	3 40 nsec	3 3/8
•	4 80 nsec	4 4/8
•	5 160 nsec	5 5/8
127 2048K	6 320 nsec	6 6/8
	7 EXT CLK	7 7/8
	(200 MHz only)	8 8/8

F(17): Enable read mode. Sets address counter to beginning of data record so that F(2) will read data properly. Must be followed by at least one F(2) or a Z.

F(19): Write to offset register. Use W1-W8 as binary input. With a grounded analog input, a code of 0 will produce an output sample of approximately 255. An offset code of 255 will produce a sample approximately equal to 0.

F(24): Disable LAM.

F(25): Computer stop trigger. Causes transient recorder to stop sampling after the selected number of post-trigger samples have been stored. Q=1 when in Ready state.

F(26): Enable LAM.

F(27): Test LAM status. Q=1 if LAM is set independent of LAM enable.

1.2.3.8 Front-Panel Description

LED Indicators

N/Power (TR8828 Series): This dual LED flashes green when CAMAC N is asserted. Red indicates all power supply voltages are present on the control board of the module.

Ready/LAM (TR8828 Series): This dual LED flashes green when the sampling clock has been enabled and the unit is digitizing and storing data. When red, it indicates that the digitizing sequence is completed and that internal LAM is set.

Power (TR8828 Series): Red LED indicates all power supply voltages are present on the ADC board of the TR8828 Series.

Power (Memory Module): This dual LED flashes green when the memory is being accessed. When red, it indicates that power is present.

SMA Connectors

INPUT: The analog input accepts 510 mV pp signals with a DC offset in the range of $\pm 1/2$ full scale. The gain accuracy is 2% of nominal (2 mV/count) with a temperature stability of $\pm 0.04\%$ of full scale per $^{\circ}\text{C}$. The analog bandwidth is greater than 100 MHz (3 dB) for amplitudes up to full scale. The input has an impedance of $50\ \Omega$, $\pm 1\%$. The input is protected from inputs with a source impedance of at least $50\ \Omega$ to $\pm 500\ \text{V}$ for 30 nsec, $\pm 100\ \text{V}$ for 100 μsec . or $\pm 2.5\ \text{V}$ continuous.

HIGH LEVEL INPUT: This input is similar to the INPUT described above. The input range is 5.10 V pp at a gain accuracy of 2%. All other parameters remain the same.

CLOCK-IN: This input is an ECL input terminated in $51\ \Omega$. Data conversion is initiated by the positive edge, accepting an input frequency of 200 MHz $\pm 1\ \text{MHz}$ with a 50% duty cycle. The input is protected against 5 A transients for 1 μsec . The clock must last 16 cycles after the last data sample so that the transfer to memory of the last 8 data bytes is completed. At the users option the $51\ \Omega$ resistor can be terminated to ground or -2 V. The unit is shipped with the ground connection.

CLOCK-OUT: This output provides an ECL compatible output of the 200 MHz clock. At the users option the ECL output may be pulled down to -5 V with a $110\ \Omega$ resistor. If no pulldown is selected, the output must be terminated externally with $50\ \Omega$ to -2 V. If the internal pulldown is selected, the output will drive $50\ \Omega$ to ground.

STOP: This input stops the sampling after the selected number of post-trigger samples have been stored. The minimum pulse duration is 8 nsec. The input is protected against 5 A

transients for 1 μ sec. The threshold can be set and monitored from the front panel. The threshold range is ± 2 V. Side-panel adjustments allow $\pm$ slope triggering and 51 Ω termination to ground or -2 V.

CDS: A low level input forces the equivalent of a CAMAC N. This input accepts TTL level signals and is pulled-up to +5 V with 1 k Ω .

FAST DAC: This output provides the reconstructed input signal. As shown in figure 1.1, this output is generated from data samples before they are stored in memory. This data appears at the selected sampling rate. The full scale range is approximately 1 V. The fast DAC output requires a 50 Ω termination to ground.

ARM BUSY: This output is a TTL open collector output indicating the status of the sampling activity of the TR8828 Series. A side-panel jumper allows selection of the polarity of this signal. When True, the TR8828 Series is sampling and waiting for a trigger.

TRIG BUSY: This output is a TTL open collector output indicating that the TR8828 Series has accepted an internal or external trigger and is acquiring the post-trigger samples. A side-panel jumper allows selection of the polarity.

MULTI-PIN CONNECTORS

Address: This 34-pin connector contains the address signals and control lines for writing to or reading from the memories. The signals are single-ended ECL except for the clock, which is differential. The address lines must be terminated by a memory module. The bus is unidirectional with the drivers in the TR8828 Series only.

Data: This 50-pin connector contains the databus from the TR8828 Series to the memory modules. The databus is 4 bytes wide, ECL, and must be terminated by a memory module. This bus is unidirectional with the drivers in the TR8828 Series only. The SPF line, indicating power-fail in the memory modules, is on this connector.

1.2.3.9 DC Linearity

DC linearity of the TR8818 is measured using the 1 million sample test discussed in Section 1.2.3.2. It is factory tested over at least 500 mV of the available 512 mV range. The test uses DC levels generated by a digital-to-analog converter in 0.5 mV steps (total of one thousand steps). At each DC level one thousand data samples are recorded. The one thousand digitized outputs are averaged to obtain a data point corresponding to a particular DC level input. After all one thousand data points have been accumulated, a best fit straight

line is determined. All TR8818 modules are adjusted so that the maximum deviation of any point from the best-fit straight line is less than two counts.

1.2.3.10 Burst Mode

In the normal mode of operation, the minimum memory size is 32k bytes and the maximum size is 2 megabytes. Active memory is a portion of physical memory defined by the user in multiples of 16k bytes. Memory cannot be read out until all of the active memory has been addressed with data or intentionally padded with "non-data".

In the "normal mode", contiguous waveform samples collected at the selected sampling rate are loaded into consecutive memory addresses. Pretrigger sampling is available from 0/8 to 8/8 of active memory.

The first and last 16 waveform samples in memory are not valid and must be rejected by the user during data interpretation or signal processing.

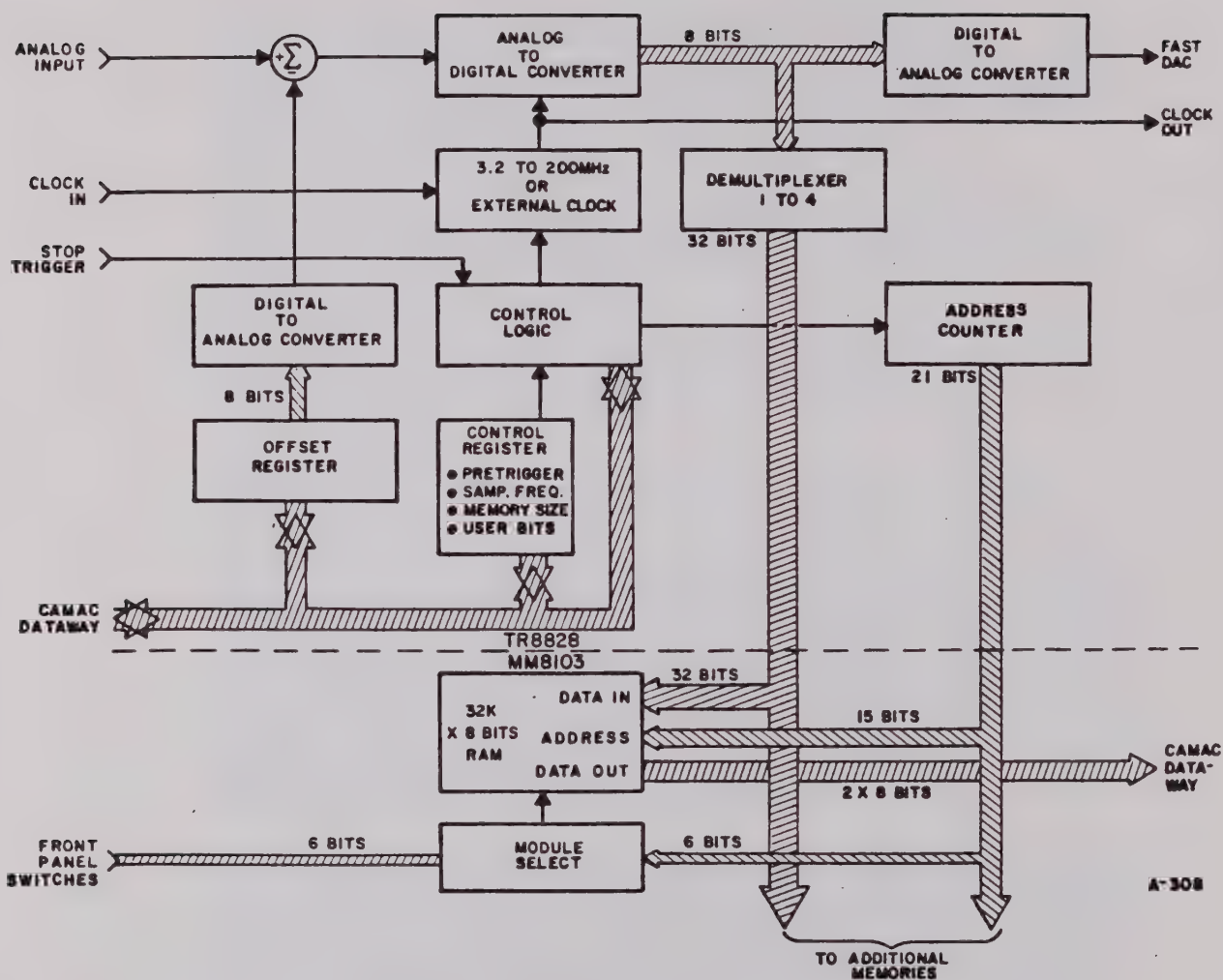
The duration of the digitized waveform depends on sampling rate and total memory employed.

Burst mode is a feature of the TR8828C only. This allows efficient use of memory when digitizing many short record segments (mode enabled with side-panel jumper). This enables the front-panel stop trigger input to double as a clock control such that data will not be transferred to memory as long as the trigger level is present. (It is recommended that a time reference pulse be injected into the high-level input at the beginning of each segment in order to identify each segment when reconstructing the data from memory.)

Active memory may be less than physical memory (same as in the normal mode). In the burst mode, contiguous waveform samples belonging to a "burst" (region of interest) are loaded into memory. By means of a burst gate (logic level), the user defines durations and times of occurrence of the regions of interest for which waveform digitizing is desired. With the stop trigger set for positive triggering and the threshold set to the desired level, a positive edge must occur before data can be taken. Data is then stored in memory when the stop trigger goes low and stops when the trigger goes high again. Opposite is true for negative triggering. See Figure 1.3

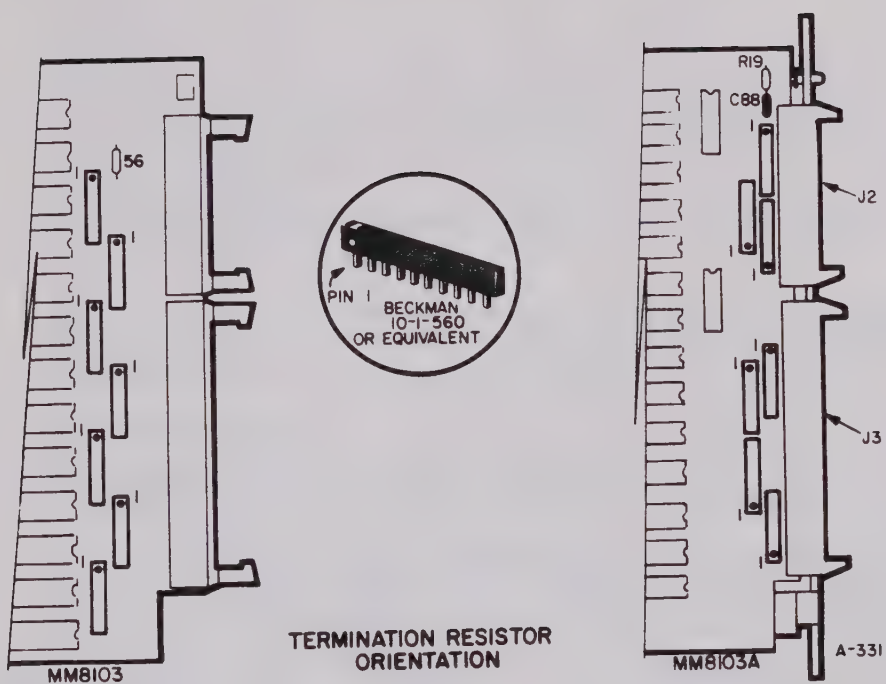
Pretriggering sampling must be set to 0/8 when using the burst mode.

The first 16 waveform samples belonging to the first burst are not valid data. Similarly, the last 16 samples belonging to the last burst must be discarded. However, 100% of the remaining waveform samples contained in all other bursts are good and valid.



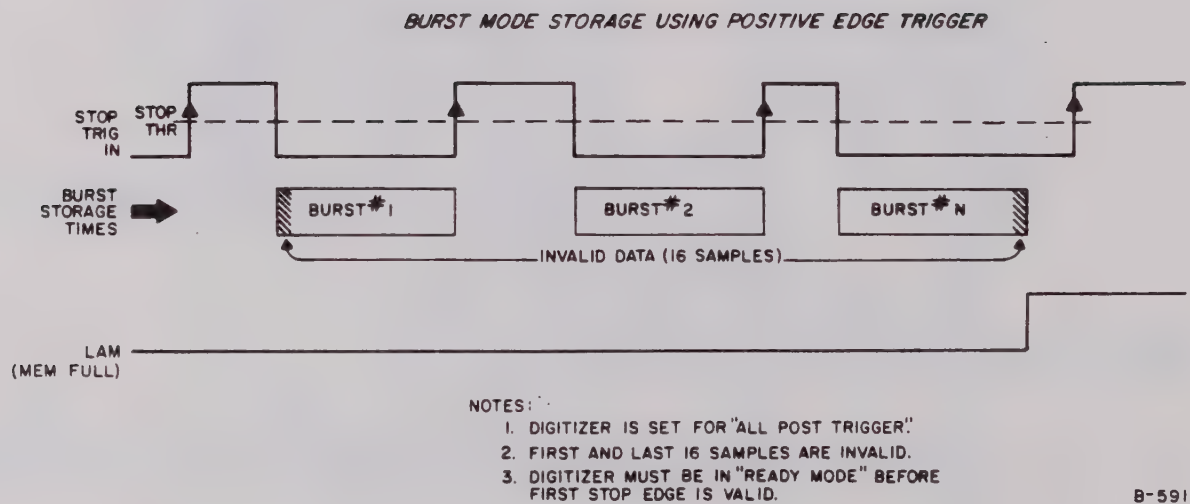
System Block Diagram

Figure 1.1



Memory Module
Termination Resistor Orientation

Figure 1.2



B-591

Figure 1.3

SECTION 2

SYSTEM OPERATION

2.1 Installation

2.1.1 Inspection

Upon receipt of the TR8828 Series and Memory system, a careful inspection of the units is recommended to insure that no damage occurred during transit.

The custom-designed shipping carton should be saved in case further shipping is necessary.

After removal from the box, the unit should be examined for physical damage. The front panel, rails, and front and rear connectors should be examined carefully.

2.1.2 Power Requirements

The TR8828 Series requires the following power supplies:

+6 V at	775	mA
-6 V at	9.0	A
+24 V at	220	mA
-24 V at	175	mA

The MM8103A/MM8104 requires:

+6 V at	2.90	A
-6 V at	1.80	A

2.1.3 Cable Requirements

The TR8828 Series requires two cables to connect the address and data buses to the memory module system memory. The 34-conductor upper cable connects the address bus while the shielded 50-conductor lower cable connects the data bus. These cables should be kept as short as possible to minimize crosstalk and reflections.

The cables are constructed with the following parts which are available through LeCroy or directly from the manufacturers as listed:

34-Conductor Cable	
Connector 34 pin	LRS #403-220-034 3-M #3414-6034
Flat Cable 34 conductor	LRS #592-030-034 3-M #Scotchflex 3365/34
50-Conductor Cable	
Connector 50 pin	LRS #403-211-050 3-M #3425-6050
Flat Cable 50 conductor	LRS #592-040-050 3-M #Scotchflex 3476/50

2.2 Operating Instructions

2.2.1 Setting Up a System

On the TR8828 Series the termination voltage of the clock and stop trigger inputs must be selected. Jumpers allow the user to select either ground or -2 V termination. The TR8828 Series is shipped from the factory with ground selected for both inputs. The side panel shows the jumpers required to select the desired option. The stop slope should be selected at this time. The CLOCK OUT internal pulldown should also be selected at this time.

The memory modules require some preparation before installation. First, the resistors which terminate the two cables must be removed from all but the last memory module on each cable. Removing all of the SIP resistor packs and the single 56 Ω resistor located in the sockets just behind the front panel accomplishes this. Now the front-panel switches must be set. These switches set the select codes in a binary fashion. Switch 1 sets the LSB and switch 5 sets the MSB. Close all the switches on all the MM8103A's. This sets the select code to 0. (A closed switch sets the bit to 0, an open switch sets the bit to 1). The first pair of MM8103A's must have a select code of 0, the next 1, the next 2, and so on until all of the MM8103A's have been given sequential select codes. Switch 6 on one module of each pair must be open and the other switch 6 of each pair must be closed.

For a single MM8104, be sure the side-panel plug option is in the proper (8104) position for single-module (high speed) operation. Then set front-panel switches 1 thru 6 to 0. If multiple MM8104's and MM8103A's are used, then the side-panel jumper should be put in the low speed (8103) mode and front-panel switches should be set as above.

For MM8105, switch 1 sets the LSB and switch 3 sets the MSB. Switch 4 on one module of each pair must be open and the other switch 4 of each pair must be closed. Switches act in the same manner as for MM8103A.

Now the TR8828 Series and memories may be placed in a CAMAC crate. The modules must be placed in the same crate, in any slots except slots 24 and 25.

After connecting the two cables between the TR8828B and memories, the crate may be powered up. Now the stop threshold may be set. The range is ± 2 V and can be set and monitored at the front panel.

NOTE: TR8828F must be used with a single MM8104.

2.2.2 Using the System

Power Up: After applying power to the transient recorder and memories, a Z (reset) command should be issued.

Setting Control Word: Because the control register has battery back-up, it will always contain the last control word written to it. When the transient recorder is not in the Ready state, the control word may be read and changed using the F(0) and F(16) CAMAC functions.

Setting Offset: The offset register is also battery backed-up and will contain the last value of offset written to it. When the transient recorder is not in the Ready state, the offset may be read or changed using the F(1) and F(19) CAMAC functions. Adjusting the offset value with F(19) allows the known input to be placed at the desired position within the 0 to 255 step output range of the digitizer.

Sampling a Waveform: Once the pretrigger, sampling period, memory size, and offset are as desired, input waveforms can be recorded. The F(9) command starts the sampling. Sampling will continue until receiving a stop trigger. There are two ways to stop the transient recorder, the CAMAC function F(25) or the stop trigger input. After the trigger, the transient recorder continues until the selected number of post-trigger samples have been digitized and stored, then the LAM is set. To determine if the sampling has finished, the LAM or LAM status can be tested with F(8) or F(27) respectively. An alternative to polling the LAM is to enable the LAM with F(26) before starting to sample and then using the crate LAM to interrupt the processor controlling the transient recorder.

Reading Waveform Data: Once the sampling is completed, the waveform data can be read. First F(17) is given to initialize the read process. F(17) must be used before any read so that the address counter is initialized and the proper data can be read. Use F(2) to read the waveform data. Data is read 16 bits at a time. The first word read, a status word, specifies which of the bytes in the next two words start the data. If the status word is a 0, then R1-R8 of the next word contain the first byte and R9-R16 contain the second byte. If the status word is a 1, then R9-R16 of the next word contain the first byte and R1-R8 of the third word contain the second byte etc. For each further use of F(2) two bytes will be returned. The first in R1-R8, the second in R9-R16. The first and last 16 bytes of the data record are garbled and should be discarded.

2.2.3 Sample FORTRAN Program

The following FORTRAN program illustrates the use of the TR8828 Series and Memory Modules:

```

1:
2: C example program for the TR8828 Series
3:
4: C the subroutine CAMO executes one CAMAC cycle
5: C the parameters for the subroutine CAMO(SLOT,F,A,W) are
6: C         SLOT      for which N is asserted
7: C         F         value of function code to be asserted
8: C         A         address to be asserted
9: C         W         data written to W1-W16
10:
11: C the subroutine CAMI executes one CAMAC cycle
12: C the parameters for the subroutine CAMI(SLOT,F,A,X,Q,R) are
13: C         SLOT      for which N is asserted
14: C         F         value of function code to be asserted
15: C         A         address to be asserted
16: C         X         value of X returned (true or false)
17: C         Q         value of Q returned (true or false)
18: C         R         data read from R1-R16
19:
20:         INTEGER SLOT, MEM, PERIOD, PRETRG, USER, CONTRL, OFFSET
21:         INTEGER PNTR, TEMP, DATA(1024)
22:         LOGICAL X, Q
23:
24: C address transient recorder in slot 10 of crate 1
25:         CALL CRATE(1)
26:         SLOT=10
27:
28: C pulse Z reset line to reset transient recorder
29:         CALL PULSEZ

```

```

30:
31:  C set memory size to 16K (range 0-31)
32:      MEM=0
33:
34:  C set sampling period to 5nsec (range 0-7)
35:      PERIOD=0
36:
37:  C set pretrigger samples to 4/8 of memory size (range 0-8)
38:      PRETRG=4
39:
40:  C set user bits to 3 (range 0-7)
41:      USER=3
42:
43:  C write to control register using F(16) and A(0) to set memory size
44:  C sampling period, pretrigger samples, and user bits.
45:      CONTRL=USER*8192+MEM*256+PERIOD*16+PRETRG
46:      CALL CAMO(SLOT,16,0,CONTRL)
47:
48:  C set input offset to center 0 V input (range 0-255)
49:      OFFSET=128
50:
51:  C write to offset register with F(19) and A(0)
52:      CALL CAMO(SLOT,19,0,OFFSET)
53:
54:  C start sampling and reset LAM with F(9) and A(0)
55:      CALL CAMO(SLOT,9,0,0)
56:
57:  C issue stop command, F(25) and A(0), then check for LAM
58:  C if LAM is not set meaning that the recorder is not finished,
59:  C then issue another stop and check LAM again...
60:
61:  C the additional stops are required because the stop trigger is
62:  C disabled during the first cycle through the memory to
63:  C insure that the pretrigger samples are written
64:
65:  100    CALL CAMO(SLOT,25,0,0)
66:          CALL CAMI(SLOT,27,0,X,Q,TEMP)
67:          IF(.NOT.Q) GOTO 100
68:
69:  C load starting address into memory address counter
70:  C and initialize data read-out with F(17) and A(0)
71:      CALL CAMO(SLOT,17,0,0)
72:
73:  C read status word to get pointer to first data byte
74:  C add 16 to pointer so that garbled bytes are skipped
75:      CALL CAMI(SLOT,2,0,X,Q,PNTR)
76:      PNTR=PNTR+16
77:

```

```
78:  C read waveform data (1024 bytes) using F(2) and A(0)
79:      DO 200 I=0,511
80:          CALL CAMI(SLOT,2,0,X,Q,TEMP)
81:  C          get data byte from R1-R8
82:          DATA(2*I+1)=TEMP.AND.255
83:  C          get data byte from R9-R16
84: 200      DATA(2*I+2)=(TEMP/256).AND.255
85:
86:  C the array DATA now contains 1024 8-bit samples
87:  C with values of 0 to 255
88:  C the PNTR points to the first valid sample
89:
90:      STOP
91:      END
```

2.2.4 GPIB Commands for Use with LeCroy 8901A

The following is a condensed outline of commands to assist a first time user of LeCroy's modular CAMAC Models TR8818 or TR8828 Series transient recorders in combination with the LeCroy Model 8901A CAMAC to GPIB interface. It is the most basic information required, just sufficient to operate the system, assuming the user is generally familiar with the GPIB controller (computer) being used. It is suggested that the individual manuals and technical data sheets on these modules as well as IEEE-583 CAMAC and 488 GPIB Standards be used if a more thorough understanding of the system is desired.

The GENERAL command set should provide all necessary information to set and read back the transient recorder parameters, to start and stop it and to read the resulting data. Use of that limited command set should be sufficient if system interrupts are not required (i.e., start Memory Readout automatically after Stop Trigger, with sufficient waiting time for any post-trigger samples to be taken).

The "INTERRUPT" command set is to be used if a "ready to read" flag is required. (See also General TR8818/TR8828 Series Information below). Either of two methods may be used:

1. Loop on INTERRUPT TEST (see table) until Response byte indicates a LAM (ready to read) is present.
Read Memory Data.
2. Send INTERRUPT ENABLE sequence. A LAM (ready to read flag from the recorder will now assert SRQ in the 8901A.
Send INTERRUPT CLEAR. Perform GPIB Serial Poll to reset SRQ.
Read Memory Data.
(This sequence is only valid for use with one transient recorder. Multiple channels may require a more complex routine.)

or

In both tables, the following notation is used:

"OUT" (or "IN" are composite commands, sometimes directly available as BASIC commands or FORTRAN calls, which set the addressed 8901A to LISTEN (or TALK), transfer data, then UNLISTEN (or UNTALK). If primitive GPIB commands are used, the 3-step sequence normally should be executed every time. (See also General 8901A Information below.)

"IN x" is required by the 8901A, as shown in the following command sequences, to execute an internal CAMAC cycle. The "x" data is not important, in fact, need not be read back.

"N" is the slot number the arrow on the recorder module front panel points to in the CAMAC crate.

"Bn" is(are) the 8-bit (0-255) data byte(s) numbered in sequence as sent or received.

"R" is a Response byte, providing X (valid command) and CAMAC Q (valid data) in the 1st and 2nd bits, respectively.

GENERAL Command Set

FUNCTION	COMMAND	COMMENTS
Set OFFSET	OUT 19,0,N,B1 IN x	See data sheet for offset table (e.g., 128 = Bipolar)
Read OFFSET	OUT 98 OUT 1,0,N IN B1,B2,R	Set 8901 for 2-byte read Set specific Read Command Read value of B2
Set MEMORY SIZE SAMPLE PERIOD, PRETRIG SAMPLES	OUT 25,0,N,B1,B2 IN x	See data sheet for Composite table (requires 2 bytes, see "TR8818/ TR8828 Series Information" below)
Read MEMORY SIZE, SAMPLE SIZE, PRETRIG SAMPLE	OUT 98 OUT 0,0,N IN B1,B2,R	Set 8901 for 2-byte read Set specific Read command Read composite value (B1+B2 form 16-bit composite word, see below)
START DIGITIZING	OUT 9,0,N IN x	Recorder storing data in memory All commands but STOP disabled
STOP DIGITIZING	OUT 25,0,N IN x	Equivalent to Stop Trigger
READ Mode Enable	OUT 17,0,N IN x	Set Memory Address to Zero, etc.
READ Two Samples	OUT 98 OUT 2,0,N IN B1,B2,R	Set 8901 for 2-byte read Set specific Read command Read value of B1,B2 (may be used to determine first sample location, see below)
READ Entire Data	OUT 106 OUT 2,0,N IN B1,B2,__,Bend,R	Set Block Transfer mode in 8901 Send Command to Read Read Data Block, (Length set by controller)

INTERRUPT COMMAND SET

FUNCTION	COMMAND	COMMENTS
INTERRUPT Enable	OUT 65 OUT 26,0,n IN x	Enables SRQ in 8901 Enables LAM in Recorder Execute
INTERRUPT Disable	OUT 24,0,N IN x	LAM will not assert SRQ but TEST still active
INTERRUPT Test	OUT 98 OUT 27,0,n IN B1,R	Set 8901 for 1-byte read Sets specific read command Read value of "R", If 2nd bit=1, LAM is present. (Ignore "B1")
INTERRUPT Clear command)	OUT 10,0,N IN x	Clears LAM. (Also Cleared by Start Digitizer

General 8901A Information

Note that the GPIB Address switch is on the front panel of the Model 8901A. It should be checked to see that it is in the desired address before installing the 8901A module.

(Caution: The 8901A does not UNTALK on a TALK to another address, it only responds to the Universal UNTALK — TALK to Address 31, or to a LISTEN command to its Address.)

The following is a complete condensed list of the available 8901 commands.

FUNCTION	DEVICE COMMANDS
Initialize all modules	33
Set for 8-bit plus status (2-byte) read	97
Set for 16-bit plus status (3-byte) read	98
Set for 24-bit plus status (4-byte) read	100
Set for High Speed block transfer 8-bit read	105
Set for High Speed block transfer 16-bit read	106
Set for High Speed block transfer 24-bit read	108
Enable SRQ on occurrence of LAM	65
Enable SRQ on occurrence of Q=0	66
Enable SRQ on occurrence of X=0	68
Disable SRQ	64

General TR8818/TR8828B Information

First Byte in Memory defines location of first valid data word (see F(2) under CAMAC Commands in appropriate Transient Recorder Technical Data sheet for details).

A 16-bit control register contains Memory Size (7-bits), Sampling Period (3 bits), Pretrigger Sample (4-bits) and one unassigned bit. Therefore, the entire 2-byte word must be created and written, even if only one of the individual parameters is being changed. (See F(0) under CAMAC Commands in appropriate Transient Recorder Technical Data sheet for the bit tables.)

The START Digitizing Command will disable all other Transient Recorder commands except STOP Digitizing. Once Digitizing is complete, commands respond normally.

End

Set for High

SECTION 3

TECHNICAL DESCRIPTION

3.1 Analog-to-Digital Converter

3.1.1 General Description

The Analog-to-Digital Converter (ADC) resides on the left hand circuit board and communicates with the Controller via an internal cable. It transmits data to memory via the front-panel data bus. Critical high-speed analog processing components are all contained in state-of-the-art thick-film hybrid circuits.

3.1.2 Technical Details

Refer to the Schematics and the block diagram in Figure 3.1. In the following description WXX-Y means device W number XX on board Y where Y is R (right hand board) or L (left hand board). The TR8828B-1 is the lefthand board and the TR8828B-2 is the righthand board.

3.1.2.1 Analog Processing

Signal inputs are routed via overload protection diodes to U11-L, the track-and-hold. This provides a gain of 5X from the INPUT and 0.5X from the HIGH LEVEL INPUT to its output. Also the offset voltage provided by the DAC (U27-R) on the controller card is summed with the input signals. Q2 provides bias current for the output stage of U11-L. U11-L output tracks the input for approximately 2.5 nsec and holds it for the remainder of the clock period.

U11-L output is routed two ways; to the input of U14-L, and to U41-L via the analog delay cable mounted on the lefthand side cover. U14-L contains the first rank (coarse) 4-bit ADC and Digital-to-Analog Converter (DAC). The output of U11-L is applied to U14-L input via a $26.1\ \Omega$ series terminator. (The signal line impedance of U14-L is $26\ \Omega$ and is internally terminated.) Full scale signal input to U14-L is $\pm 0.64\text{ V}$, corresponding to $\pm 1.28\text{ V}$ at U11-L output. Adjustable reference voltages for U14-L ADC are provided by U22-L and R79-L; its DAC reference voltage is provided by U4-L, Q1-L and R89-L.

The DAC output of U14-L and the delayed analog signal from U11-L are subtracted and amplified in U41-L, a d.c. coupled amplifier with sub-nanosecond risetime. The signal at U41-L output corresponds to the difference between U11-L output and the analog equivalent of the first rank data. It is applied via series terminator R91-L to the second rank (fine) ADC, U54-L, where the second 4-bit conversion takes place. The adjustable reference voltage for U54-L is provided by U65-L and R112-L. R87-L provides adjustment of second rank offset. Q4-L provides bias current for U41-L output stage. U42-L, U55-L, and U57-L are pipeline latches for temporary storage of U14-L data until U54-L data is available.

3.1.2.2 Digital Processing

The digital processing provides three basic functions: clock generation and selection, byte stacking and byte dropping. Some sections of the controller circuits reside on the ADC circuit board; this avoids the transmission of clocks and data between ADC and controller at greater than 50 MHz.

The internal clock oscillator consists of Q3-L and Y1-R, a 100 MHz fifth overtone quartz crystal. U17-L converts the clock signal to ECL levels and doubles the clock frequency to 200 MHz. U15-L selects internal or external clock and converts the output of the clock filter back to ECL levels. The clock filter is a pair of coupled tuned circuits designed to eliminate phase jitter due to harmonic or sub-harmonic components of the clock. U19-L and U27-L buffer and fan out the clock.

Clock pulses to the first and second rank ADC's, pipeline latches and clock dividers are generated in the correct phase by high-quality twisted-pair delay cables and differential line receivers. The track-and-hold clock is buffered by U9-L, filtered and phase-shifted by the TR8828B-4 circuit board, and applied to the differential clock inputs of U11-L via an unbalanced-to-balanced transformer, T3-L. R31-L via CR9-L through CR11-L controls the phase and therefore the timing of U11-L clock signal.

The final output of the clock pipeline U19-L is divided by U25-L, U27-L, U29-L to produce the data clock at various sampling rates. U13-L, U20-L and U21-L decode the control signals F4, F5 and F6 which are transmitted via the internal cable from the controller card to select the desired sampling rate or the external clock. U27-L fans the data clock out to the address counter (U35-L), the post-trigger counter (U37-L) and the byte stacker (U59-L, U60-L, U61-L, U62-L). The counters are split between the ADC card and the controller card, thus scaling the 200 MHz sampling clock to 50 MHz before transmitting it to the controller card via the internal cable. AD1 clocks the address counters and PT1 clocks the post-trigger counters on the controller card.

The scalers U35-L and U37-L only operate when the system is writing to memory. When not writing to memory the data generated by the ADC is ignored. When U33-L and U51-L are set to start the scaling of the address counter, the latch clock to the byte stacker (U66-L, U68-L, U70-L, U72-L, U74-L, U76-L) begins transmitting data via the 50-conductor cable to the memories. The byte stacker accumulates 4 bytes before transmitting them to the memory. Dropping data samples in the byte stacker allows the TR8828B to sample at lower sampling rates.

When a stop command is received, either via the front-panel connector and stop comparator (U53-L) or the CAMAC function code F(25) and A(0) as decoded by the controller board, the flip flop U46-L is clocked which then enables the post-trigger counter and the clock to the controller card PT1. When the post-trigger samples have been taken the two LSB's of the address counter are latched by U50-L and saved on the controller card as the start address. Also at this time the write signal to the controller is negated. The address counter and post-trigger counter scalers are then reset and disabled until the next sampling command, F(9) and A(0) is received by the controller.

3.2 Digital Controller

3.2.1 General Description

The controller portion of the TR8828 Series resides on the righthand board and communicates with the ADC board through a 20-conductor cable connecting the two. The controller board is called the TR8828B-2 board.

Logic consisting of ECL, CMOS, and TTL is used to minimize power dissipation and maximize performance. ECL is used in the address counter, post-trigger counter, and fast control logic. Registers that are backed up by batteries are CMOS. The rest of the logic is low power Schottky TTL.

CAUTION: Unsolder the battery before attempting to repair this unit.

3.2.2 Technical Details

NOTE: In the following description UXX-Y means IC number UXX on board Y where Y is R (righthand board) or L (lefthand board).

3.3.32.2.1 CAMAC Control

A(0), N, and NOT F4 are decoded by U34-L. U41-L uses the output of U34-L and the remaining F lines to decode the commands accepted by the TR8828 Series. An X and Q response is generated for all commands by U3-L. Since most commands generate these responses, X and Q are inhibited by those commands that require X=0 and Q=0. Q is inhibited by the inputs to U104-L. X is inhibited by the inputs to U3-L.

Commands that latch data do so at the time of S1. These commands are AND'd with S1 to produce the appropriate strobes. S2 is used to increment the address counter when reading data so it is AND'd with F(2). F(17) and S2 loads the starting address of the data into the address counter, sets the valid data flip flop, and sets the first byte flip flop. F(9) and S2 sets the TR8828 Series into the digitizing or ready state. F(25) and S2 starts the post-trigger counter by enabling PT1 on the TR8828B-1 board.

Read commands enable open collector drivers onto the CAMAC read lines. All the registers that can be read by CAMAC must have their signals translated to TTL levels. Low power comparators (LM339s) are used as translators.

Write data from CAMAC is translated to the control registers with LM339 comparators. The registers use -0.8 V and -5.2 V for power with VDD at -0.8 V and VSS at -5.2 V. CMOS can drive ECL logic directly if these supplies are used.

3.2.2.2 Memory Control

Figure 3.2 is a block diagram of the logic that controls the addressing of memory. The memory is organized as a circular file of data samples. There are two operating modes for the memory control, write to memory and read memory.

Write to memory is initiated by F(9) and A(0). The flip flops U46-L, U51-L are set to wait for the stop. The flip flops U33-L, U51-L are set to start the scaling of the address counter and to generate a write to the memory. During the WRITE mode the one's complement of the memory size is multiplexed to the data inputs of the address counters. The address counter counts up to terminal count, reloads the one's complement of the memory size, and proceeds to count up again. Therefore, memory is loaded with data at addresses starting at full scale - memory size up to an address of full scale -1. This cycle is repeated until a STOP is received.

STOP starts the post-trigger counter. When the write to memory is initiated, F(9) and A(0) loads the post-trigger counter with the one's complement of the memory size and the fraction or pretrigger size. The post-trigger counter is two counters in series. One (U37-L, U76-R, U77-R, U78-R, U79-R) counts up to the memory size divided by 16 repetitively and the second (U80-R) counts to the fraction multiplied by 16 once. The overall effect is to count the post-trigger samples. At the terminal count of the post-trigger counter, WRITE is negated. In addition not WRITE sets the internal LAM flip flop U95-R. The data can now be read from memory.

Asserting F(17) and A(0) loads the starting address from the CMOS latch into the address counter and loads the memory size and zero pretrigger into the post-trigger counter. VALID DATA flip flop U95-R and FIRST BYTE flip flop U96-R are also set. The first assertion of F(2) and A(0) will put B0 and B20 onto the R1 and R2 lines of the CAMAC dataway. This is the status word, indicating the position of the start byte in the 2 byte words that are read from memory. The second and successive F(2)'s increment the address counter and the post-trigger counter by two. Scaling by two occurs because both flip flops in U75-R are enabled, which enables clocks to the second bit of both counters. The memory modules places 2 bytes onto the read lines of the CAMAC dataway for every read clock. When terminal count is reached in the post-trigger counter, VALID DATA is negated and further F(2)'s will generate a Q=0 response.

3.2.2.3 ADC Control

Offset is supplied to the ADC via connector J4. An 8-bit DAC (U27-R) produces a current which flows through a resistor (R15-R) and a potentiometer (R14-R). The resultant voltage is buffered by U20-R. A CMOS register (U29-R) stores the offset value when F(19) and A(0) are asserted. Asserting F(1) and A(0) will enable the stored word via U28-R onto the R9 through R16 lines of the CAMAC dataway.

3.2.2.4 Power Fail and Battery Backup

Power failure in the controller card is detected by monitoring three of the power supplies used by the card. Zener diodes, resistors, and an opto isolator detect the presence of the +24 V supplies. A series string of resistors and LED's check the -6 V supply. The result of these checks are AND'd together to produce POWERON. SPF from the ADC and memories is translated and AND'd with POWERON to enable the X response. Failure of any supply will disable the X response.

Battery backup is accomplished with battery B1-R and diode CR5-R. Resistor R2-R is used to monitor current when the power is off. When a power fail is detected all register clock inputs are held high and tri-state outputs are disabled. Capacitors C15-R, C32-R, and C34-R maintain the logic supplies at their nominal levels while the power fail logic turns everything off.

The -2 V supply is distributed between two regulators and fanned out to the 100 Ω pull downs with ten individual wires from E11-R through E20-R.

3.3 Memory

3.3.1 General Description

Memory modules contain sixteen 2K x 8 CMOS STATIC RAM IC's or sixteen 8K X 8 CMOS STATIC RAM IC's for MM8105. Read and write cycle time for these IC's is 120 nsec in MM8103A and MM8105, 70 nsec in MM8104. At the maximum data rate 4 bytes appear at the front panel every 40 nsec. These 4 bytes are assembled into an 8-byte word which is presented simultaneously to an upper bank of eight memory IC's and a lower bank of eight memory IC's. Only one bank gets a write pulse for each 8-byte word. Thus, the worst case minimum cycle time is 160 nsec in MM8103A and MM8105, 80 nsec in MM8104, much slower than the cycle time of the memory IC's.

CAUTION: Unsolder one lead of the battery or remove jumper E1-E2 before attempting repairs on this unit.

3.3.2 Technical Details

3.3.2.1 WRITE Cycle

Address and data lines are terminated with removable 100 Ω SIP resistors. The differential clock line is terminated with a single 100 Ω removable resistor. Of the twenty address lines received by the memory the upper six address lines are used as module select lines. These six lines are compared with the front-panel switches to determine if the module is selected. Exclusive OR's perform this function, generating the signal called SEL which enables appropriate gates in the module. Figure 3.3 is a block diagram.

Both the upper bank and lower bank see their address and data inputs from similar sources. This ensures symmetric operation with respect to the address and databus. Address and data latches for both banks accomplish this symmetric operation. Figure 3.4 shows the timing of address, data, and write enable at each memory bank. The data is common to both banks, strobed only at the appropriate time.

Once a write cycle has started the cycle is completed independent of the state of the SEL line. This is important when more than one module is in a system. As the address bus deselected one module and selects another, the previous write cycle to the last bank must be completed. Write cycles overlap from one module to the next because of pipelining of data within the modules.

Flip flops in U56 control the timing of the write enable pulses to the memory IC's. Clocks are delayed appropriately with gates in U65. Note that signals UBDI and LBDI are not enabled by SEL. This ensures a full-width write enable as long as the clock and address lines continue to toggle.

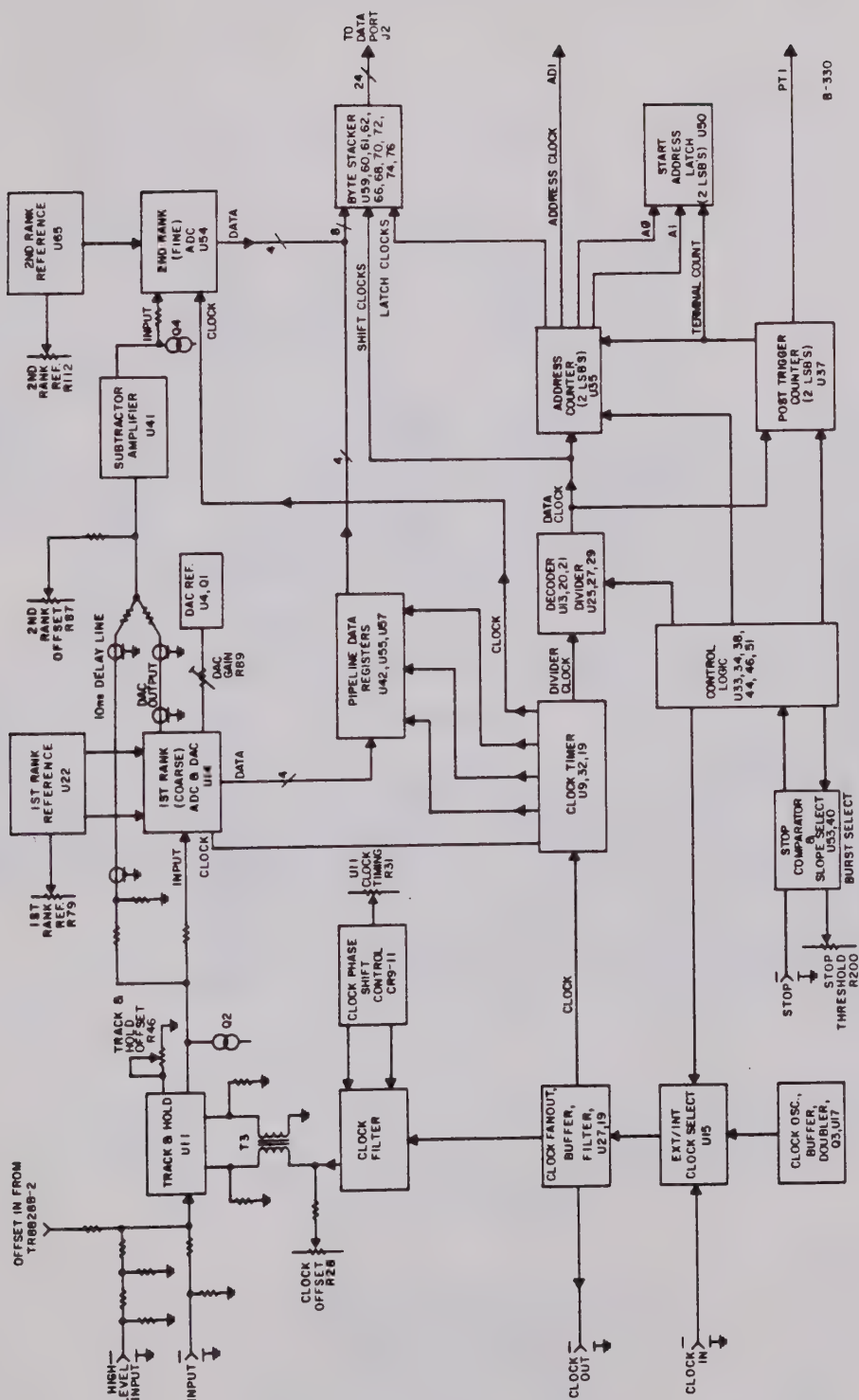
3.3.2.2 READ Cycle

During the read cycle AB1, AB2, and AB3 are decoded to read 2 bytes at a time from the sixteen memory IC's. Open collector drivers put the bytes onto the R1 through R16 read lines of the CAMAC dataway.

The READ line is simply the decoded F(2) and A(0) from the transient recorder. The address changes near the end of the CAMAC cycle when S2 increments the address in the transient recorder. This address change before the end of the READ cycle will create a short enable pulse from the decoders.

3.3.2.3 Power Fail and Battery Backup

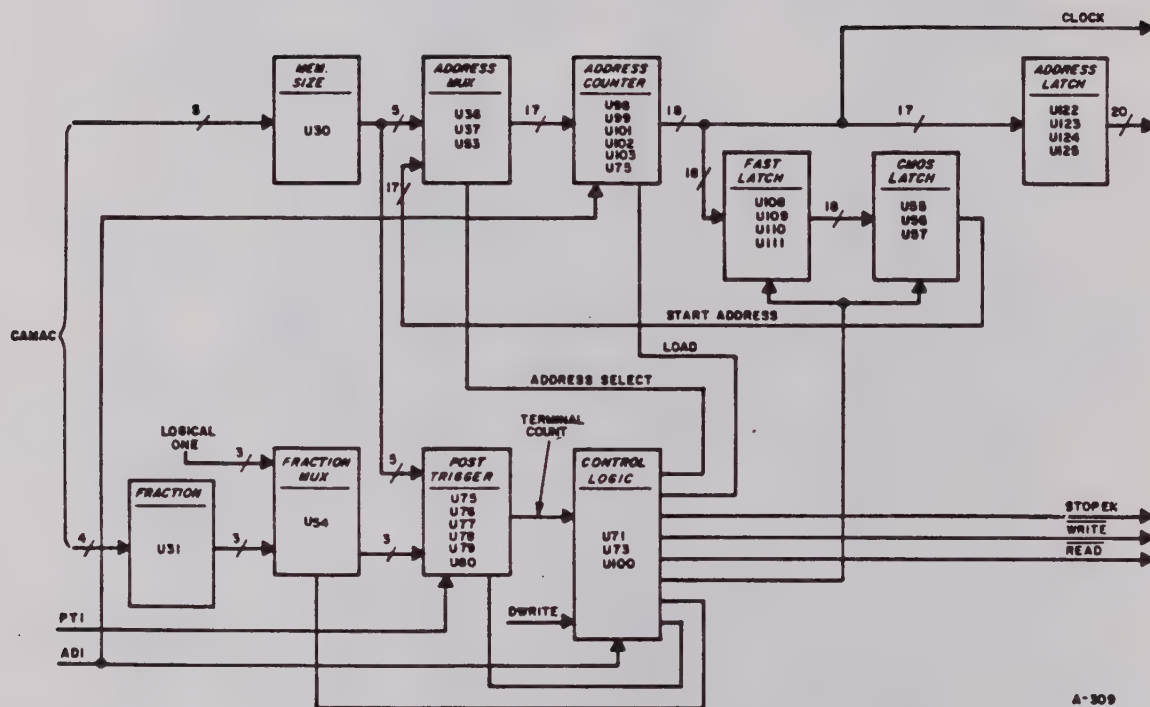
The two power supplies are sensed with a series string of diodes and a resistor. As long as +5.2 V is available the red LED will be enabled and SPF will be low. Loss of power will turn off the red LED and pull SPF to -.08 V. SPF is driven by an open emitter and must have a pull-down in the transient recorder. On power fail the battery maintains the data in the CMOS memories. Chip select is held high when power is off. Pull-downs to ground on the address lines keep the current requirements of the memory IC's to a minimum during power fail. Resistor R1, in series with the battery, is used to measure the current drain from the battery when the power is off. When the battery is installed the current is measured to ensure a typical five-year lifetime of the battery.



BLOCK DIAGRAM TR8828B ADC CARD

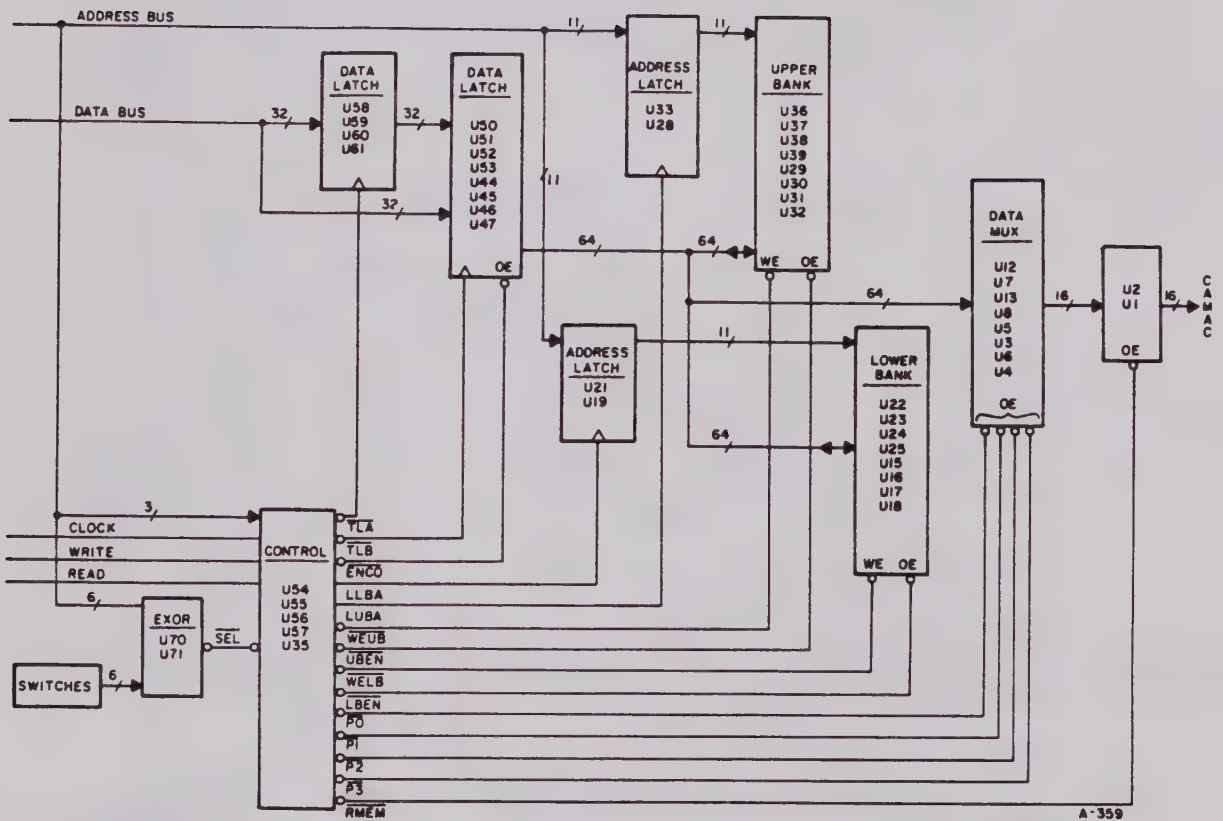
Block Diagram TR8828 ADC Card

Figure 3.1



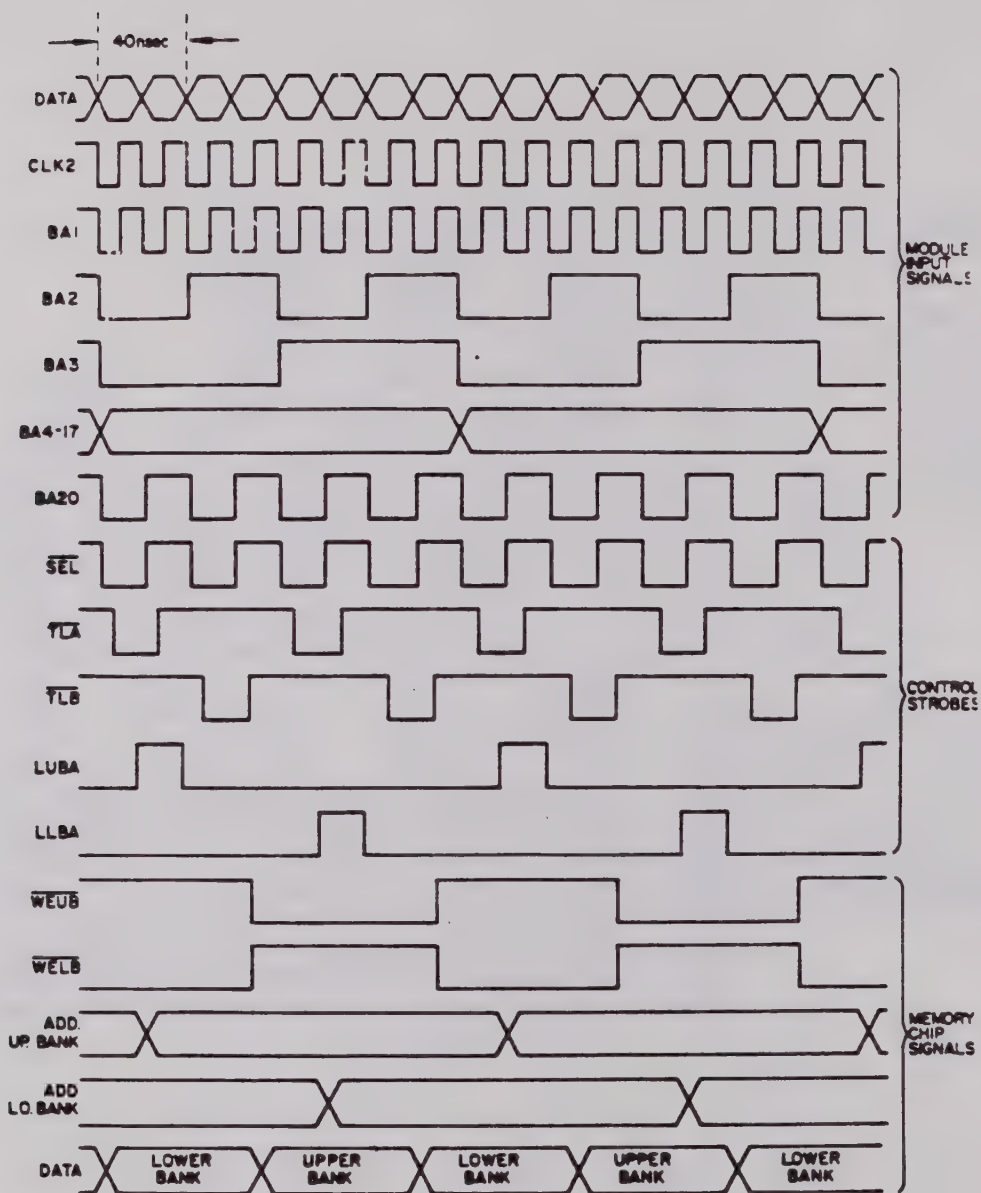
Controller Block Diagram
TR8828 Series

Figure 3.2



Memory Block Diagram

Figure 3.3

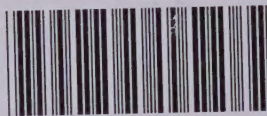


B-307

Memory Timing Signals for
TR8828 Series

Figure 3.4

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